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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,459	12/16/2003	Chien-Hsien Kao	11461-US-PA	1458

31561 7590 06/02/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,459	KAO ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: the square brackets of the title should be deleted.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahara et al (US 5,436,635, Takahara) in view of Sekine (US 6,181,312).

4. As to claim 1, Takahara teaches a first embodiment of a liquid crystal panel [see Figs. 1 and 3], comprising:

a panel [a LCD panel, Fig. 3], having a plurality of pixels [pixels P_{11} through P_{mn}], wherein each one of the pixels includes a first transistor [a transistor T_{p11}] and a second transistor [a transistor T_{m11}];

a first group of gate lines [G_{p1} through G_{pn}], coupled to each the first transistor [T_{p11}] at a gate electrode ; a second group of gate lines [G_{m1} through G_{mn}], coupled to

each the second transistor [T_{m11}] at a gate electrode [see a first embodiment, col. 13, line 19 through col. 15-16, line 46]; and

a first group of source lines [S_{p1} through S_{pn}, see col. 13, line 19 through col. 15-16, line 46].

Accordingly, Takahara teaches all of the claimed limitation, except wherein one of the first group of gate lines and the second group of gate lines can be used to feed with gate pulse signals with respect to an actual image data and the other one can be used to with gate pulse signals with respect to a black image data.

However, Sekine teaches a LCD device which includes one of odd [$(2a+1)^{th}$, a is natural numbers] group of gate lines and even [$(2b^{th})$, b is natural numbers] group of gate lines can be used to feed with gate pulse signals with respect to an central picture area [see Figs. 1 and 13, col. 11, lines 38-44], and the other one can be used to with gate pulse signals with respect to the top and bottom black areas [see Figs. 1 and 13, col. 9, lines 58-63, and col. 11, lines 50-61 for further operating of the gate drive circuit].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the group of gate pulses with respect to the central picture area and the other group of gate pulses with respect to the top and bottom black areas as taught by Sekine for using to drive with the first and second groups of gate electrodes, respectively in the LCD device of Takarara, because this would improve the quality of the image being displayed, while fabricating the driving circuitry with a smaller circuit scale and easier [see Sekine, col. 13, lines 15-33].

5. As to claim 2, Sekine teaches the liquid crystal panel of claim 1, wherein the gate pulse signals are fed by a time difference to the first group of gate lines and the second group of gate lines [Fig. 13 of Sekine expressly shows the gate pulses G_1 through G_{2N} are shifting in different timing].

6. As to claim 3, Takahara teaches the liquid crystal panel of claim 1, wherein input terminals of the first group of gate lines and the second group of gate lines are located at the different sides of the panel [see Fig. 1].

7. As to claim 4, Sekine teaches the liquid crystal panel of claim 1, wherein the first group of source lines can be fed with the actual image data [see col. 11, lines 10-12].

8. As to claim 5, Takahara teaches the liquid crystal panel of claim 1, wherein drain electrodes of the first transistor [T_{p11}] and the second transistor [T_{m11}] are coupled to a terminal of a capacitor [a pixel electrode plate P_{11} and an electrode plate V+ make up a capacitor, see Fig. 1].

9. As to claim 6, the combination of Takahara and Sekine teaches the liquid crystal panel of claim 1, further comprising: a second group of source lines [a source line IC (M) 12, see Takahara's Fig. 1, col. 16, lines 28-34 for further modifying of the source line IC], wherein one of the first group of source lines and the second group of source lines can be fed with the actual image data, and the other one can be fed with the black image data [Sekine teaches one of odd [$(2a+1)^{th}$, a is natural numbers] group of gate lines and even [$(2b^{th})$, b is natural numbers] group of gate lines can be used to feed with gate pulse signals with respect to a central picture area, see Sekine's Figs. 1 and 13, col. 11, lines 38-44, and the other one can be used to with gate pulse signals with

respect to the top and bottom black areas, see Sekine's Figs. 1 and 13, col. 9, lines 58-63, and col. 11, lines 50-61].

10. As to claim 7, Sekine teaches the liquid crystal panel of claim 6, wherein the actual image data and the black image data are fed by a time difference [Fig. 13 of Sekine expressly shows the group of gate pulses G_1-G_{2a} at a timing T_{w1}, and the group of gate pulses G_{2a+1}-G_{2b} at a timing T_s, the timing T_{w1} and T_s are different].

11. As to claim 8, Takahara teaches the liquid crystal panel of claim 6, wherein drain electrodes of the first transistor [T_{p11}] and the second transistor [T_{m11}] are coupled to a terminal of a capacitor [a pixel electrode plate P_{11} and an electrode plate V+ make up a capacitor, see Fig. 1].

12. As to claim 9, Takahara teaches a first embodiment of a driving device for a liquid crystal display (LCD) panel [see Figs. 1 and 3], the driving device comprising:

a liquid crystal (LC) panel [Fig. 3] ;

a first gate driver [a gate drive (P) 13, Fig. 1], having a first gate circuit, coupled to the LC panel;

a second gate driver [a gate drive (N) 14, Fig. 1], having a second gate circuit, coupled to the LC panel; and

a first source driver [a source drive IC (P) 11, Fig. 1], having a first source circuit, coupled to the LC panel.

Accordingly, Takahara teaches all of the claimed limitation, except wherein one of the first group of gate lines and the second group of gate lines can be used to feed

with gate pulse signals with respect to an actual image data and the other one can be used to with gate pulse signals with respect to a black image data.

However, Sekine teaches a LCD device which includes one of odd [$(2a+1)^{th}$, a is natural numbers] group of gate lines and even [$(2b^{th})$, b is natural numbers] group of gate lines can be used to feed with gate pulse signals with respect to an central picture area [see Figs. 1 and 13, col. 11, lines 38-44], and the other one can be used to with gate pulse signals with respect to the top and bottom black areas [see Figs. 1 and 13, col. 9, lines 58-63, and col. 11, lines 50-61 for further operating of the gate drive circuit].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the group of gate pulses with respect to the central picture area and the other group of gate pulses with respect to the top and bottom black areas as taught by Sekine for using to drive with the first and second groups of gate electrodes, respectively in the LCD device of Takarara, because this would improve the quality of the image being displayed, while fabricating the driving circuitry with a smaller circuit scale and easier [see Sekine, col. 13, lines 15-33].

13. The limitation of claim 10 is the same as those of claim 2 and therefore the claim will be rejected using the same rationale.

14. The limitation of claim 12 is the same as those of claim 4 and therefore the claim will be rejected using the same rationale.

15. The limitation of claim 14 is the same as those of claim 6 and therefore the claim will be rejected using the same rationale.

16. The limitation of claim 15 is the same as those of claim 7 and therefore the claim will be rejected using the same rationale.

17. Claims 11, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahara in view of Sekine as applied to claim 9 above, and further in view of Kang (US 6,621,547).

The combination of Takahara and Sekine teaches all of the claimed limitation, except for the limitation of claim 11 recites "wherein each of the first gate driver and the second gate driver comprises: a shift register, coupled to receive an input signal; a level shifter, coupled to the shift register; an output buffer, coupled to the level shifter and the corresponding gate circuit, wherein the first gate driver and the second gate driver are located at the same side or at the different sides of the LC panel; wherein when the first gate driver and the second gate driver are located at the same side, the first gate driver and the second gate driver can be a same one of driver or different drivers;"

for the limitation of claim 13 recites "wherein the first source driver comprises: a digital to analog converter (DAC), coupled to receive a data input; and an output buffer, coupled to the DAC and the first source circuit;" and

for the limitation of claim 16 recites "wherein each of the first source driver and the second source driver comprises: a digital to analog converter (DAC), coupled to receive a data input; and an output buffer, coupled to the DAC and the first source circuit, wherein the first source driver and the second source driver are located at the same side or at the different sides of the LC panel; wherein when the first source driver

and the second source driver are located at the same side, the first source driver and the second source driver can be a same one of driver or different drivers;"

For the limitation of claim 11, Kang teaches a LCD device which includes each of the first gate driver [332a, Fig. 4] and the second gate driver [332b, Fig. 4] comprises: a shift register [332a Fig. 3], coupled to receive an input signal; a level shifter [332b, Fig. 3], coupled to the shift register; an output buffer [332c, Fig. 3] coupled to the level shifter and the corresponding gate circuit, wherein the first gate driver and the second gate driver are located at the same side of the LC panel [Fig. 3]; wherein when the first gate driver and the second gate driver are located at the same side, the first gate driver and the second gate driver can be a same one of driver [see col. 7, lines 25 through col. 8, line 44 for further operating of the gate driving IC(s) 332];

For the limitation of claim 13, Kang teaches the driving device of claim 9, wherein the first source driver [322a, Fig. 4] comprises: a digital to analog converter (DAC) [322b, Fig. 3], coupled to receive a data input; and an output buffer [322c, Fig. 3], coupled to the DAC and the first source circuit [see col. 6, lines 14-22 for further operating of the data driving IC(s) 322];

For the limitation of claim 16, Kang teaches the driving device of claim 14, wherein each of the first source driver [322a, Fig. 4] and the second source driver [332b, Fig. 4] comprises: a digital to analog converter (DAC) [322b, Fig. 3], coupled to receive a data input; and an output buffer [322c, Fig. 3], coupled to the DAC and the first source circuit, wherein the first source driver and the second source driver are located at the same side of the LC panel; wherein when the first source driver and the

second source driver are located at the same side, the first source driver and the second source driver can be a same one [see col. 6, lines 14-22 for further operating of the data driving IC(s) 322].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the gate driving IC(s) and the data driving IC(s) in the combination of Takahara and Sekine with the gate driving IC(s) [332] and the data driving IC(s) [322] including the shift register [332a], the level shifter [332b], the buffer [332c], DAC [322b], and the buffer [322c], respectively as taught by Kang, because this would improve high resolution of the image being displayed [see Kang, col. 8, lines 19-44], while reducing volume occupied by gate printed circuit boards or medium for transmitting gate-driving signals to gate lines and weight thereof [see Kang, col. 1, line 65 through col. 2, line 8].

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KMN
May 26, 2006

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Patent Examiner
Art Unit 2629